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Description

INTERFACE APPARATUS USING SINGLE DRIVER, COMPUTER SYSTEM INCLUDING INTERFACE APPARATUS USING SINGLE DRIVER, AND RELATED METHOD

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to interface control, and more particularly, to a apparatus using a single driver, a computer system including an apparatus using a single driver, and a related method.

[0003] 2. Description of the Prior Art

[0004] Within computer systems nowadays, buses are essential, for example: ISA, PCI, PCI EXPRESS. Peripheral devices complying with the bus specification have become very popular. In order to save the number of interface slots occupied within a computer system, products such as interface cards are often implemented having multiple inter-

face devices to meet end-user requirements.

[0005] Each interface device on the interface card requires a driver, which is a control program adaptive to the computer system where the interface card is installed. If one of the interface devices of the interface card needs the cooperation of another of the interface card, the two drivers for both interface devices involved and an additional driver for controlling the two drivers are required. Furthermore, if parameters related to calculations of both interface devices need to be transferred between the two interface devices, programmers will be required to add this functionality to the drivers and to debug these drivers while programming. As a result, programming the drivers of the multiple interface devices of the interface card is more complicated than programming a driver of a single interface device.

SUMMARY OF INVENTION

[0006] It is therefore an objective of the present invention to provide an interface apparatus using a single driver, a computer system including an interface apparatus using a single driver, and a related method to solve the above-mentioned problem.

[0007] The present invention provides an interface apparatus

coupled to a bus, the interface apparatus including: a first controller for performing a logic operation, wherein when a processor coupled to the bus initializes the interface apparatus, the first controller is enabled to respond a message to the processor for indicating that the interface apparatus is a single-function device; and a second controller coupled to the first controller for performing a logic operation, wherein when the processor initializes the interface apparatus, the second controller is disabled; wherein when the processor disables the first controller, the second controller is allowed to communication with the processor through the first controller.

[0008] The present invention correspondingly provides a computer system comprising: a processor for controlling operations of the computer system; a bus coupled to the processor for transmitting data; and an interface apparatus coupled to the bus including: a first controller for performing a logic operation, wherein when the processor initializes the interface apparatus, the first controller is enabled to respond a message to the processor for indicating that the interface apparatus is a single-function device; and a second controller coupled to the first controller for performing a logic operation, wherein when the

processor initializes the interface apparatus, the second controller is disabled; wherein when the processor disables the first controller, the second controller is allowed to communication with the processor through the first controller.

[0009] The present invention correspondingly provides a method for using a bus in the computer system which comprises a processor and an interface device, the interface device comprising a first controller and a second controller, the method comprising: generating a first message to indicate that the interface device is a single-function device when the interface device is initialized; generating a second message to request a total memory volume including a first portion that will be utilized by the first controller and a second portion that will be utilized by the second controller; and determining which one of the first controller and the second controller responds to the processor according to a command from the processor.

[0010] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0011] Fig.1 is a block diagram of a computer system according to one embodiment of the present invention.

[0012] Fig.2 is a block diagram of a computer system according to another embodiment of the present invention.

[0013] Fig.3 is a block diagram of a computer system according to another embodiment of the present invention.

Detailed Description

[0014] Please refer to Fig.1 illustrating a block diagram of a computer system 100 according to a first embodiment of the present invention. In this embodiment, the computer system 100 includes a PCI interface card 110, a PCI bus 130 coupled to the PCI interface card 110 for transmitting data, and a processor 150 coupled to the PCI bus for controlling operations of the computer system 100. The PCI interface card 110 includes a first controller 112-1 labeled as PCI Device 1 in Fig.1 for performing a logic operation and a second controller 112-2 labeled as PCI Device 2 in Fig.1 for performing a logic operation.

[0015] In this embodiment, the first controller 112-1 includes a core circuit 116 for performing the logic operation of the first controller 112-1. The code 116c within the core cir-

cuit 116 is the program code for performing the logic operation of the first controller 112-1.. The first controller 112-1 further includes a register 113 for storing a flag used to control whether the first controller 112-1 or the second controller 112-2 is enabled. The first controller 112-1 further includes a selecting module 114 coupled to the register 113. In the embodiment, the selecting module 114 couples to the core circuit 116 via REQB1_IN, GNTB1_IN, and IDSEL1_IN. Please note, the REQB1_IN, GNTB1_IN, and IDSEL1_IN are in accordance with the PCI specification.

[0016] As shown in Fig.1, the selecting module 114 further includes a REQB pin REQB1, a GNTB pin GNTB1, and an IDSEL pin IDSEL1. Please note, the pins REQB1, GNTB1, and IDSEL1 are in accordance with the PCI specification and are well known in the art. The second controller 112-2 further includes a REQB pin REQB2, a GNTB pin GNTB2, and an IDSEL pin IDSEL2, all coupled to the selecting module 114. Please note, the pins REQB2, GNTB2, and IDSEL2 are in accordance with the PCI specification and are well known in the art. When the first controller 112-1 is enabled, the selecting module 114 connects the pins REQB1, GNTB1, and IDSEL1 to the REQB1_IN, GNTB1_IN, ID-

SEL1_IN, respectively. When the second controller 112-2 is enabled, the selecting module 114 connects the pins REQB1, GNTB1, and IDSEL1 to the pins REQB2, GNTB2, and IDSEL2, respectively.

[0017] As shown in Fig.1, the first controller 112-1 further includes an INTB pin INTB1. In addition, the second controller 112-2 further includes an INTB pin INTB2 coupled to the pin INTB1 of the first controller 112-1. Furthermore, each of the controllers further includes a set of pins 118 coupled to the PCI bus 130. In the embodiment, the pins 118 includes: a plurality of address pins AD[31:0], a Frameb pin, an Irdyb pin, and a Trdyb pin, ... , etc., all in accordance with the PCI specification and being well known in the art.

[0018] As a result of the connection illustrated in Fig.1, only a single driver adaptive to the computer system 100 is required for controlling all the PCI devices, specifically the controllers 112-1 and 112-2, within the PCI interface card 110. According to an initial value of the flag stored in the register 113, when the processor 150 initializes the PCI interface card 110, the first controller 112-1 is enabled and responds with a message to the processor 150 to indicate that the PCI interface card 110 is a single-function

device. At this time, the second controller 112-2 is disabled. In addition, when the processor 150 initializes the PCI interface card 110, the first controller 112-1 responds with a message to the processor 150 for requesting a total memory volume (A+B) including a first portion A that will be utilized by the first controller 112-1 and a second portion B that will be utilized by the second controller 112-2. That is, the memory-based address of the first controller 112-1 is set for accessing the total memory volume (A+B) but the first controller 112-1 only utilizes the first portion A.

[0019] According to the first embodiment shown in Fig.1, when a PCI scan is performed, there is a message sent to the first controller 112-1 through the pin IDSEL1, but there is no message sent from the first controller 112-1 to the second controller 112-2 through the pin IDSEL1. Therefore, only the first controller 112-1 is responsible for PCI configurations when the PCI interface card is initialized. After the driver is started, the processor 150 executing the driver is capable of replacing the initial value of the flag stored in the register 113 with another value to enable the second controller 112-2 and disable the first controller 112-1. When the the second controller 112-2 is enabled,

the second controller 112-2 is allowed to communicate with the processor 150 through the first controller 112-1. In this situation, the pins REQB2, GNTB2, and IDSEL2 of the enabled controller 112-2 are coupled to the pins REQB1, GNTB1, IDSEL1, respectively, while the core circuit 116 within the first controller 112-1 is isolated. Then, during a PCI configuration of the second controller 112-2, the memory-based address of the second controller 112-2 is set for accessing the second portion B.

[0020] After this, the driver may send commands to the first controller 112-1 or the second controller 112-2 as needed. The first controller 112-1 identifies any DMA access of the second controller 112-2 as required and sends a corresponding message to the second controller 112-2 for controlling the DMA access. If there are any interrupts generated by the first controller 112-1 or the second controller 112-2, the driver will be notified since the pins INT1 and INT2 are coupled.

[0021] The present invention correspondingly provides a method for using the PCI bus. The method is already disclosed above and is summarized as follows.

[0022] Step 10:Provide the PCI interface card 110 coupled to the PCI bus 130, wherein the PCI interface card 110 includes

the first controller 112-1 and the second controller 112-2.

[0023] Step 20:When the PCI interface card 110 is initialized, enable the first controller 112-1 to respond with a message to the processor 150 coupled to the PCI bus 130 to indicate that the PCI interface card 110 is a single-function device.

[0024] Step 30:When the PCI interface card 110 is initialized, disable the second controller 112-2.

[0025] Step 40:When the second controller 112-2 is enabled, allow the second controller 112-2 to communicate with the processor 150 through the first controller 112-1 and the PCI bus 130.

[0026] Fig.2 illustrates a block diagram of a computer system 200 according to a second embodiment of the present invention. As shown in Fig.2, a PCI interface card 210 of the computer system 200 includes components 212-1, 212-2, 213, 214, 216, and 218, which are similar to the components 112-1, 112-2, 113, 114, 116, and 118 of the computer system 100, respectively. The PCI interface card 210 further includes a third controller 212-3. In the second embodiment, when the first controller 212-1 is enabled, the selecting module 214 connects the pins

REQB1, GNTB1, and IDSEL1 to the REQB1_IN, GNTB1_IN, and IDSEL1_IN, respectively. In addition, when the second controller 212-2 is enabled, the selecting module 214 connects the pins REQB1, GNTB1, and IDSEL1 to the pins REQB2, GNTB2, and IDSEL2, respectively. Furthermore, when the third controller 212-3 is enabled, the selecting module 214 connects the pins REQB1, GNTB1, and IDSEL1 to the pins REQB3, GNTB3, and IDSEL3, respectively. As connections of the third controller 212-3 within the PCI interface card 210 are similar to that of the second controller 212-2, and as the register 213 is for storing a flag to ensure that one of the controllers 212-1, 212-2, and 212-3 is enabled at a time, the operations of the second embodiment will not be repeated.

[0027] Fig.3 illustrates a block diagram of a computer system 300 according to a third embodiment of the present invention. As shown in Fig.3, a PCI interface card 310 of the computer system 300 includes components 312-1, 312-3, 313-1, 314-1, 316-1, and 318, which are similar to the components 112-1, 112-2, 113, 114, 116, and 118 of the computer system 100, respectively. The PCI interface card 310 of the computer system 300 further includes components 312-2, 313-2, 314-2, and 316-2,

which are similar to the components 312-1, 313-1, 314-1, and 316-1, respectively, with the exceptions described as follows. As shown in Fig.3, the pins REQB2, GNTB2, and IDSEL2 of the selecting module 314-2 are coupled to the selecting module 314-1, and the pins REQB3, GNTB3, and IDSEL3 of the third controller 312-3 are coupled to the selecting module 314-2. A flag stored in the register 313-2 is used to control whether either the second controller 312-2 or the third controller 312-3 is enabled if the first controller 312-1 is disabled. When the second controller 312-2 is enabled, the selecting module 314-2 connects the pins REQB2, GNTB2, and IDSEL2 to the pins REQB2_IN, GNTB2_IN, and IDSEL2_IN of the core circuit 316-2, respectively. In addition, when the third controller 312-3 is enabled, the selecting module 314-2 connects the pins REQB2, GNTB2, and IDSEL2 to pins REQB3, GNTB3, and IDSEL3, respectively. Furthermore, when either the second controller 312-2 or the third controller 312-3 is enabled, the selecting module 314-1 connects the pins REQB1, GNTB1, and IDSEL1 to the pins REQB2, GNTB2, and IDSEL2, respectively.

[0028] It is an advantage of the present invention method and device that when the PCI interface card is initialized, the

first controller is enabled to respond with a message to the processor to indicate that the PCI interface card is a single-function device and the other controller(s) is disabled. As a result, only a single driver is needed for controlling the PCI interface card.

[0029] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.